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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,332	07/30/2003	Hyesook Hong	TI 35165	8758

23494 7590 11/16/2009

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EXAMINER	
POMPEY, RON EVERETT	

ART UNIT	PAPER NUMBER
2812	

NOTIFICATION DATE	DELIVERY MODE
11/16/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

Office Action Summary	Application No.	Applicant(s)	
	10/630,332	HONG ET AL.	
	Examiner	Art Unit	
	RON POMPEY	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/30/09*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18,20 and 21* is/are pending in the application.

4a) Of the above claim(s) *1-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-18 and 20-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 9-18 and 20-21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kent (US 6130016), in view of Krivokapic et al. (US 5646870) and further in view of Minobe et al. (US 7304791).

Kent discloses the limitations of:

In re Claim 9: providing a reticle layer over a reticle substrate, said reticle layer including each of:

a patterned feature area (lower row of widely spaced patterns 220, fig. 3a) corresponding to a desired circuitry pattern; and

a test pattern area (upper row of closely spaced patterns 220, fig. 3a), wherein a portion of said test pattern area is within a step-distance of a portion of said patterned feature area (col. 6, lns. 14-40);

patterning a resist material by stepping said reticle, the patterning including each of the patterned feature area and test pattern area incorporated in said reticle layer; and

visually inspecting said material within said test pattern area, said light and dark regions representing a corresponding variance in said patterned feature area of the resist material. (col. 6, ln. 45 – col. 7, ln. 51)

In re Claim 10: wherein said portion of said test pattern area (upper row of closely spaced patterns 220, fig. 3a) is a first portion of said test pattern area and said portion of said patterned feature area (lower row of widely spaced patterns 220, fig. 3a) is a first portion of said patterned area and wherein said first portion of said test pattern area is within a step-distance of said first portion of said patterned feature area and a second portion of said test pattern area is within a step-distance of a second portion of said patterned feature area, a variance between said first and second portions of said test pattern area being indicative of a variance between said first and second portions of said patterned area (fig. 4B);

In re Claim 11: wherein said test pattern area creates a reflective grating in said patterned resist material and said reflective grating is configured to provide said light and dark regions if said variance in said patterned feature area exists (fig. 4B; col. 7, lns. 9-51);

In re Claim 12: wherein said reflective grating includes a reoccurring line/space structure (patterned photoresist/metal; col. 7, ln. 1-40);

In re Claim 15: wherein said variance is a systematic variance in critical dimension (CD) in said test pattern area (cd = linewidth; col. 6, lns. 1-10) ;

In re Claim 18: patterning a resist material by stepping a reticle, wherein said reticle includes each of:

a patterned feature area (lower row of widely spaced patterns 220, fig. 3a) corresponding to a desired feature of a semiconductor device; and

a test pattern area (upper row of closely spaced patterns 220, fig. 3a), wherein a portion of said test pattern area is within a step-distance of a portion of said patterned feature area; and

visually inspecting said patterned resist material within a corresponding test pattern area, said light and dark regions representing a systematic variance in critical dimension (CD) in said patterned resist material (fig. 4b);

using said patterned resist material to form the feature of a semiconductor device after said visually inspecting (col. 6, ln. 45 – col. 7, ln. 51).

In re Claim 20: wherein said patterned resist material is used to form multiple features, and wherein said multiple features are electrically contacted to form an operational integrated circuit (col. 6, lns. 1-6).

In re Claim 21: (New) A method for making a semiconductor device, comprising:

patterning a resist material using a reticle having a plurality of step areas within the reticle, wherein said reticle includes each of:

a patterned feature area (lower row of widely spaced patterns 220, fig. 3a) corresponding to a desired feature of a semiconductor device; and

a test pattern area (upper row of closely spaced patterns 220, fig. 3a), wherein a portion of said test pattern area is within a step-distance of a portion of said patterned feature area; and

visually inspecting said patterned resist material a systematic variance in critical dimension (CD) in said patterned resist material.

3. Kent reads on the claims as applied above, but does not disclose the claimed limitation(s) of:

In re Claims 9, 18 and 21: using said resist material as patterned by said reticle to form the feature of a semiconductor device after said visually inspecting.

In re Claim 14: wherein said test pattern area is located in a scribe region defined by said patterned feature area.

However,

a. Krivokapic discloses the above claimed limitations regarding:

In re Claim 9: using said resist material as patterned by said reticle to form the feature of a semiconductor device after said inspecting (209, fig. 2; wherein the patterned resist is measured and then sent to the etch 104; the further processing after the measurement completed includes the etching of station 104, col. 9 ,lns. 16-44).

In re Claim 14: wherein said test pattern area is located in a scribe region (108, fig. 4) defined by said test pattern area (col. 13, lns. 51-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the inspecting/measuring of the test pattern (In re Claim 9) in Kent with the inspecting/measuring of the resist test pattern before etching with the

resist as a mask as taught by Krivokapic because measuring the resist patterned resist will provide for accuracy maintaining the critical dimensions of the device.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify where the test pattern is placed (In re Claim 14) in Kent with placing the test pattern area in the scribe region as taught by Krivokapic because allow you to use more of the wafer for the actual devices.

4. Kent and Krivokapic read on the claims as applied above, but does not disclose the claimed limitation(s) of:

In re Claims 9 and 18: visually inspecting said material for light and dark regions within said test pattern area, said light and dark regions representing a corresponding variance in said patterned feature area of the resist material.

In re Claim 16: wherein visually inspecting said material includes visually inspecting said material using an optical microscope; and

In re Claim 17: further including changing a focus on said optical microscope to cause said light and dark regions to become more or less pronounced.

In re Claims 21: visually inspecting said patterned resist material for light and dark regions, differences in said light and dark regions between said plurality of step areas representing a systematic variance in critical dimension (CD) in said patterned resist material.

However,

b. Minobe discloses the above claimed limitations regarding:

In re Claims 9, 18 and 21: visually inspecting said material for light and dark regions within said test pattern area, said light and dark regions representing a corresponding variance in said area of the material (col. 8, lns. 16-22).

In re Claim 16: wherein visually inspecting said material includes visually inspecting said material using an optical microscope (col. 8, lns. 16-22); and

In re Claim 17: further including changing a focus on said optical microscope to cause said light and dark regions to become more or less pronounced in (col. 7, lns. 25-31).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Kent and Krivokapic with Minobe, because the optical microscope helps inspect a patterned material, which Kent is silent about how the inspection/analyze of resist is done.

2. Kent, Krivokapic and Minobe read on the claims as applied above, but **does not** disclose the claimed limitation(s) of:

In re Claim 13: wherein said reoccurring line/space structure has a pitch of less than about 3/2 a wavelength used in said patterning step;

However, it would have been obvious to one of ordinary skill in the art at the time the invention to form test pattern areas with reoccurring line/space structure that has a pitch of less than about 3/2 the wavelength in use, since it has been held that where the general conditions, the width of the lines in the reoccurring line/space structure, of a claim are disclosed in prior art, discovering the optimum or working ranges involves only

routine skill in the art. (see In re Aller,105 USPQ 233.) Because the pitch of the test pattern area will help find variances visually.

Response to Arguments

3. Applicant's arguments with respect to claims 9-18 and 20, received June 30, 2009, have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RON POMPEY whose telephone number is (571)272-1680. The examiner can normally be reached on 9AM - 5PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Walter L. Lindsay, Jr./
Primary Examiner, Art Unit 2812

/R. P./
Examiner, Art Unit 2812
AU: 2812
11/09/09